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Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2020.3014572

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Submodule Capacitance Monitoring Strategy for Phase-Shifted Carrier Pulse-Width Modulation Based Modular Multilevel Converters

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Abstract- The capacitance monitoring is one of the important issues for the MMC to obtain high reliability. Since the pulse-width modulation (PWM) is usually implemented in the Field Programmable Gate Array (FPGA), the produced precise switching states in the FPGA cannot be directly access by the top Digital Signal Processor (DSP) controller, which poses challenges on the existing capacitance monitoring methods based on the precise switching states of the MMC. This paper presents a submodule (SM) capacitance monitoring strategy for the MMC with a simple algorithm, where the fundamental frequency components of the SM capacitor voltage and current are extracted to estimate the SM capacitance based on reference, but not the precise switching states. The proposed scheme not only simplifies the implementation and calculation, but also avoids control limitations and heavy communication burden between DSP and FPGA. Besides, the proposed strategy effectively eliminates noise impact from sensors and increases accuracy. Simulation and experimental studies are implemented, and the results confirm the effectiveness of the proposed strategy.

***Index terms*—Capacitance monitoring, modular multilevel converters, reliability, PSC-PWM, submodule**

I. INTRODUCTION

The modular multilevel converter (MMC) has drawn considerable interests due to its advantages of modularity, scalability, high efficiency, low harmonic content and fault tolerance [1]-[3]. A multilevel voltage can be synthetized with the operation of the MMC and the SM switching frequency can be reduced without compromising the power quality [4]. Recently, the MMC is more attractive for renewable energy integration, medium-voltage motor drives, and electric railway supplies [5]-[7].

The capacitor is one of the fragile components in the MMC [8]. Due to high energy density and low price [9], the electrolytic capacitor is popular for MMCs in some applications, such as micro-grids, motor drives and front-end rectifier [10]-[12]. Owing to vaporization of the electrolyte, the capacitor would gradually deteriorate and capacitance would be changed [13]. Normally, the capacitor is required to be replaced with a new one when its capacitance drops below 80% of rated value [14]. As a result, it's essential to monitor the SM capacitance value for reliable operation.

Recently, several SM capacitance monitoring methods have been reported for MMCs, which can be divided into direct monitoring methods and indirect monitoring methods. The direct monitoring methods are based on precise capacitor voltage and current. Reference [15] presents a direct capacitor monitoring method for the MMC, where each SM capacitance is estimated by a recursive least square (RLS) algorithm. However, an ac current is required to be injected into the circulating current in [15], which increases the arm current and affects the MMC performance. In [16]-[19], the SM capacitance is estimated using band-pass filters and root mean square (RMS) calculations. However, a double frequency circulating current injection is required in [16] and the methods in [17]-[19] are only suitable for the MMC without circulating current suppression control (CCSC). Besides, the Kalman filter (KM) algorithm [20] and fast-affine projection (FAP) algorithm [21] are adopted to estimate the SM capacitance in MMCs. In [22], a new non-contact current sensor is implemented to extract the SM capacitor current and RLS algorithm is adopted to estimate the capacitance. The direct monitoring methods in [15]-[21] are based on capacitor voltages, arm current and SM switching states, whose estimation errors are usually below 1%. However, in some applications, the precise switching states cannot be directly access by the controller, thus the methods in [15]-[21] would have trouble in practical application.

The indirect monitoring methods are other solutions for capacitance estimation in the MMC, which are based on the relationships among the SM capacitances. Reference [23] estimates the capacitance based on the relationship between the arm average capacitance and the capacitance of each SM. Reference [24] presents a reference SM (RSM) based capacitance monitoring method to reduce computational burden, where the reference SM is employed to estimate the capacitances in other SMs. Reference [25] presents an improved RSM based capacitance estimation method, which makes full use of the voltage sensor measurement range to improve accuracy. However, two SMs have to be out of service during the monitoring period. Reference [26] presents

This work was supported in part by the National Natural Science Foundation of China under Project 61873062 and in part by the Natural Science Foundation of Jiangsu Province under Project BK20180395. *(Corresponding author: Fujin Deng.)*

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2020.3014572, IEEE Transactions on Industrial Electronics

a sorting-based capacitance monitoring method to reduce computational burden in the MMC with a large number of SMs, where only the SM with the smallest capacitance is judged and estimated. In [27], the monitored SM is controlled to be bypassed from the arm and the capacitor is discharged through the bleeding resistor, where the time of the capacitor voltage decreasing to a predefined value is used to estimate the SM capacitance. Reference [28] presents a capacitance monitoring method based on the relationship between phase current and capacitor voltage, but only during the DC-side start-up procedure. Reference [29] presents a capacitance monitoring method for MMCs with nearest level modulation (NLM) based on the relationship between SM voltage variation and SM driving signal angle. In indirect methods, the precise switching states of the SMs are not required, thus the indirect methods are easier to implement than the direct methods.

For the MMC system with a number of SMs, the typical implementation architecture is composed of the DSP and FPGA. The DSP is normally used to implement the control algorithm, while the FPGA is used to produce the switching states based on the modulation references received from the DSP. The existing capacitor monitoring methods require the precise SM switching states [15]-[21]. It means that the DSP is required to receive the precise SM switching states produced in the FPGA for the implementation of capacitor monitoring algorithm in the DSP, which would be difficult for the DSP to have such a high sampling speed and such a large calculation amount.

In this paper, a SM capacitance monitoring strategy is proposed for the phase-shifted carrier (PSC) pulse-width modulation (PWM) based MMC, where the fundamental frequency components of SM capacitor voltage and current are extracted to estimate the SM capacitance. The advantages of the proposed strategy are: 1) It does not require SM switching states, but only the references. It can be directly implemented in the DSP controller, avoid fast sampling and transmission of precise switching states from FPGA to DSP controller, and greatly reduce computational burden in comparison with [15]-[21]. 2) It has the feature of noise immunity, which increases the accuracy of the capacitance monitoring in comparison with [24] and [27]. 3) It has no extra control or effect on control performance and is more practical for implementation in comparison with [15], [17], [24] and [27].

The rest of the paper is organized as follows. Section II introduces the basic principles of the MMC. The proposed SM capacitance monitoring strategy is presented in Section III. And the discussion of the proposed strategy is presented in Section IV. Then, simulation studies and experimental studies are respectively given in Section V and Section VI to verify the effectiveness of the proposed capacitance monitoring strategy. Finally, the conclusions are drawn in Section VII.

II. Modular Multilevel Converters

Fig. 1(a) shows a three-phase MMC, which consists of phase A, phase B and phase C. The subscript u refers to the upper arm while the subscript l refers to the lower arm. Each phase is composed of an upper arm and a lower arm, which contains an arm inductor L_s and n identical SMs in series. Fig. 1(b) shows the diagram of the i-th SM in the upper arm of phase A, which is composed of upper switch/diode T_1/D_1, lower switch/diode T_2/D_2, and the capacitor C_{aui}. In normal operation, the SM is controlled by a switching function S_{aui}, as

$$S_{aui}=\begin{cases}1, & T_1 \text{ is switched on and } T_2 \text{ is switched off}\\ 0, & T_1 \text{ is switched off and } T_2 \text{ is switched on}\end{cases}. \quad (1)$$

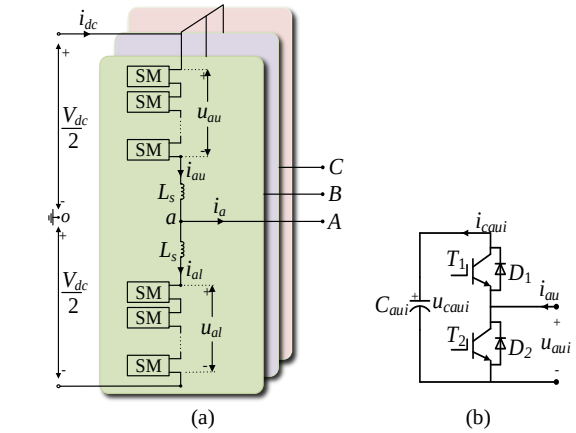

Fig. 1. (a) Three-phase MMC. (b) The i-th SM in upper arm of phase A.

III. Proposed Capacitance Monitoring Strategy For MMCs under PSC-PWM

A. PSC-PWM Based Control System of MMCs

Fig. 2 shows a typical implementation architecture for the MMC based on DSP and FPGA [30], [31]. The DSP mainly realizes control algorithm such as output current control, voltage balancing control, CCSC, capacitance monitoring, protection and user interface based on the signals such as capacitor voltages, arm currents and grid voltages received from the FPGA. Based on the produced reference signal from the DSP, the FPGA generates the switching signals for each SM based on the PWM scheme.

In the DSP shown in Fig. 2, the arm reference y_{au} is generated based on the output current control such as the active power, reactive power and dc-link voltage regulation. To guarantee each capacitor voltage balancing, the PSC-PWM

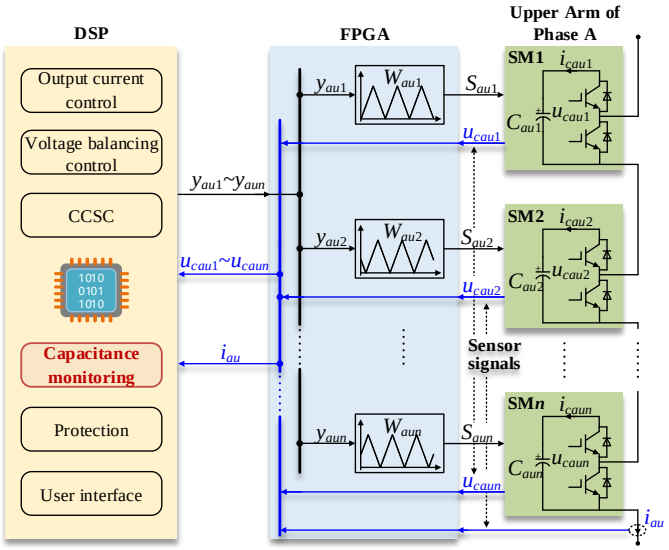

Fig. 2. Typical implementation architecture of MMCs based on DSP and FPGA.

based individual capacitor voltage balancing control is implemented. Owing to that the semiconductor stress and the power absorbed by the SMs are evenly distributed in the MMC under PSC-PWM, each SM capacitor voltage can be easily kept balanced [31]. According to [31], the balancing compensation component Δy_{aui} (i=1, 2…n) for the i-th SM is generated as

$$\Delta y_{aui} = K_p \cdot (u_{ave\_a} - u_{caui}) \cdot i_{cir\_a} \tag{2}$$

where K_p is the proportional gain, u_{ave_a} is the average capacitor voltage within phase A, i_{cir_a} is the circulating current in phase A as $i_{cir\_a}=(i_{au}+i_{al})/2$ and i_{al} is the lower arm current in phase A. As a result, the reference y_{aui} for the i-th SM is

$$y_{aui} = y_{au} + \Delta y_{aui} \tag{3}$$

The n references y_{au1}~y_{aun} are sent to the FPGA by communication. In the FPGA, n triangular carriers W_{au1}~W_{aun} are generated, which are respectively shifted by $2\pi/n$. By comparing the references y_{au1}~y_{aun} with the carriers W_{au1}~W_{aun}, respectively, the n switching functions S_{au1}~S_{aun} are generated to drive SM1~SMn in the upper arm of phase A.

B. Analysis of Capacitor Voltage and Current

In the MMC, the current in phase A can be expressed as

$$i_a = I_m \sin(\omega_0 t + \varphi) \tag{4}$$

where I_m is the peak value, ω_0 is the fundamental angular frequency and $\omega_0=2\pi f_0$, f_0 is the fundamental frequency and φ is the power factor angle. Suppose the second-order harmonic circulating current is suppressed by the CCSC [32], according to [33], the upper arm current i_{au} in phase A can be expressed as

$$i_{au} = \frac{i_a}{2} + \frac{i_{dc}}{3}. \tag{5}$$

where i_{dc} is the dc-link current of the MMC.

The voltage reference for phase A can be defined as

$$u_{a\_ref} = U_m \cos(\omega_0 t + \delta). \tag{6}$$

where U_m is the peak value and δ is the angle between the reference voltage and grid side voltage. The reference voltage for the upper arm of phase A is

$$u_{au\_ref} = \frac{1}{2} V_{dc} - u_{a\_ref} \tag{7}$$

where V_{dc} is the dc voltage, as shown in Fig. 1(a). As a result, the arm reference for the upper arm of phase A is

$$y_{au} = \frac{u_{au\_ref}}{V_{dc}} = \frac{1}{2} - \frac{M}{2}\cos(\omega_0 t + \delta). \tag{8}$$

where M is modulation index given as $M = 2U_m/V_{dc}$.

According to (5) and (8) [33], the capacitor current i_{caui} in the i-th SM is

$$i_{caui} = y_{aui} \cdot i_{au}. \tag{9}$$

The capacitor voltages u_{caui} in the i-th SM is

$$u_{caui} = u_{caui0} + \frac{1}{C_{aui}} \int_0^t i_{caui} \cdot dt, \tag{10}$$

where u_{caui0} is the dc component of capacitor voltage.

Fig. 3(a) shows the amplitudes of the fundamental frequency component and double frequency component of capacitor current under various active power; Fig. 3(b) shows the amplitudes of the fundamental frequency component and double frequency component of capacitor voltage under various active power, whose parameters are derived from simulations in Section V. It can be observed that the fundamental frequency components in capacitor current and voltage are obviously larger than the double frequency components.

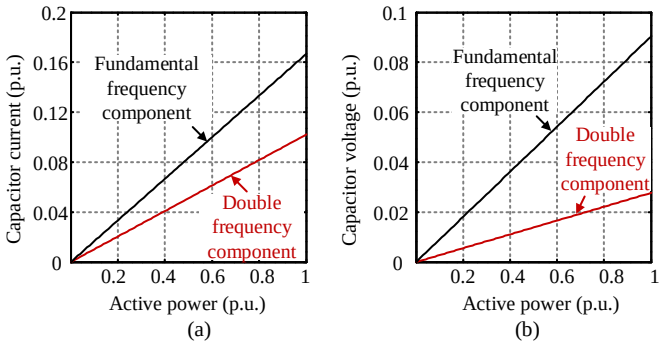

Fig. 3. Fundamental frequency components and double frequency components under various active power. (a) Capacitor current. (b) Capacitor voltage.

C. Analysis of SM Capacitance

According to the above analysis, the fundamental frequency components at angular frequency ω_0 in capacitor voltage and current are dominant, which can be used for capacitance analysis. The capacitor voltage u_{caui} in (10) is multiplied by $\cos(\omega_0 t)$ and $\sin(\omega_0 t)$, respectively, and integrated in N_T fundamental periods as

$$\begin{cases} A_{u\_aui} = \int_0^{N_T T} u_{caui}(t) \cdot \cos(\omega_0 t) dt \\ B_{u\_aui} = \int_0^{N_T T} u_{caui}(t) \cdot \sin(\omega_0 t) dt \end{cases}, \tag{11}$$

where N_T is the number of monitoring periods. T is fundamental period and T=1/f_0. The voltage coefficient F_{u_aui} is defined as

$$F_{u\_aui} = \sqrt{A_{u\_aui}^2 + B_{u\_aui}^2}. \tag{12}$$

From (11), it can be observed that when the capacitor voltage is multiplied by $\cos(\omega_0 t)$ or $\sin(\omega_0 t)$, the relationship would be as follows.

- The components in the capacitor voltage except the fundamental frequency component become alternating components, which would be eliminated in the integral process;
- The component at fundamental frequency in capacitor voltage becomes direct component, which would be accumulated in the integral process.

As a result, F_{u_aui} is only related to the fundamental frequency component in the capacitor voltage.

Similarly, the capacitor current is respectively multiplied by $\cos(\omega_0 t)$ and $\sin(\omega_0 t)$, respectively, and integrated in N_T fundamental periods as

$$\begin{cases} A_{i\_aui} = \int_0^{N_T T} i_{caui}(t) \cdot \cos(\omega_0 t) dt \\ B_{i\_aui} = \int_0^{N_T T} i_{caui}(t) \cdot \sin(\omega_0 t) dt \end{cases}, \tag{13}$$

The current coefficient F_{i_aui} is defined as

$$F_{i\_aui} = \sqrt{A_{i\_aui}^2 + B_{i\_aui}^2}. \tag{14}$$

According to (9)~(14), the SM capacitance can be estimated as

$$C_{aui} = \frac{F_{i\_aui}}{\omega_0 \cdot F_{u\_aui}}. \tag{15}$$

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D. Proposed Capacitance Monitoring Strategy

Based on the above analysis, a capacitance monitoring strategy is proposed, as shown in Figs. 4 and 5, which is implemented in the DSP controller shown in Fig. 2. In the proposed capacitance monitoring method, the capacitors in the arm are monitored one by one.

Figs. 4 and 5 show the proposed capacitance monitoring strategy for the i-th SM in the upper arm of phase A. The capacitor voltage u_{caui}, arm current i_{au} and grid voltage e_a, e_b, e_c are sampled in real-time. The phase angle θ and angular ω_0 of the grid side voltage are obtained by a phase locked loop (PLL) [34]. Suppose the monitoring command is given during the period between $(j\text{-}1)T$ and jT, the proposed capacitance monitoring algorithm will be implemented since jT and lasts for N_T periods, as shown in Fig. 4.

Fig. 5 shows the implementation of the proposed capacitance monitoring algorithm for the i-th SM in the DSP controller, where the reference y_{aui} is derived based on the system control of the MMC. After implementation of the proposed algorithm, the A_{u_aui}, B_{u_aui} and A_{i_aui}, B_{i_aui} can be calculated based on (11) and (13), respectively. At the end of the implementation of the proposed algorithm, as shown in Fig. 4, the voltage coefficient F_{u_aui} and current coefficient F_{i_aui} can be calculated based on (12) and (14). Then, the capacitance C_{aui} in the i-th SM can be estimated based on (15).

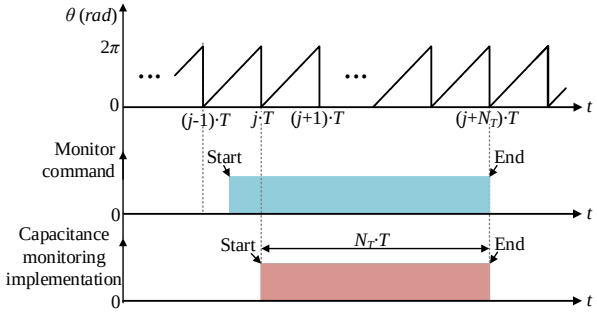

Fig. 4. Diagram of the start and end of the proposed capacitance monitoring strategy.

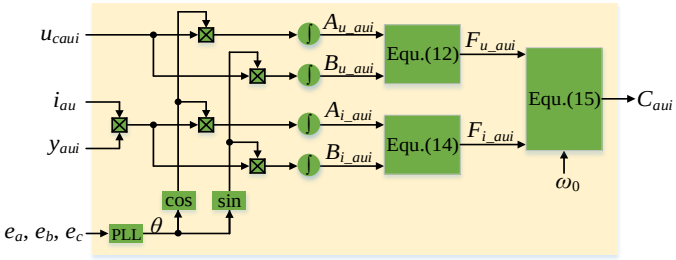

Fig. 5. Proposed capacitance monitoring strategy for the i-th SM in the upper arm of phase A.

IV. Discussion of Proposed Capacitance Monitoring Strategy

A. Analysis of Noise Immunity

To estimate the capacitances in the MMC, a large number of sensors are used for voltages and currents sampling. The measurement error is unavoidable, which would lead to inaccuracy of condition monitoring. Normally, the measurement errors mainly contain systematic errors and random errors. The systematic errors can be corrected by proofreading and compensation [35]. However, the random errors are usually caused by a variety of complex internal and external interferences during the measurement process, which are hard to avoid. The random error involved may affect the accuracy of the capacitance monitoring. Thus, the impact of the measurement error on the proposed capacitance monitoring strategy requires further investigations.

The DSP is a discrete-time controller. Considering the noise effect in a practical MMC system, the sampled i-th SM capacitor voltage $\hat{u}_{caui,k}$ and arm current $\hat{i}_{au,k}$ at the k-th control period can be respectively expressed as

$$\begin{cases} \hat{u}_{caui,k} = u_{caui,k} + v_{i,k} \\ \hat{i}_{au,k} = i_{au,k} + w_k \end{cases}, \tag{16}$$

where $v_{i,k}$ and w_k are the random errors of measurement, which can be modelled as Gauss noise with the feature of being zero-mean, white and uncorrelated [36]. $v_{i,k}$ and w_k obey normal distribution as

$$\begin{cases} v_{i,k} \sim N(0, \sigma_v^2) \\ w_k \sim N(0, \sigma_w^2) \end{cases}, \tag{17}$$

where σ_v^2 and σ_w^2 are the variance of $v_{i,k}$ and w_k, respectively. The signal-noise ratio (SNR) of the sampled capacitor voltage $\hat{u}_{caui,k}$ and current $\hat{i}_{au,k}$ are

$$\begin{cases} SNR = 20 \cdot \lg \dfrac{RMS(\hat{u}_{caui,k})}{\sigma_v} \\ SNR = 20 \cdot \lg \dfrac{RMS(\hat{i}_{au,k})}{\sigma_w} \end{cases}, \tag{18}$$

where RMS is the root mean square. Along with increase of the SNR, the noise is reduced.

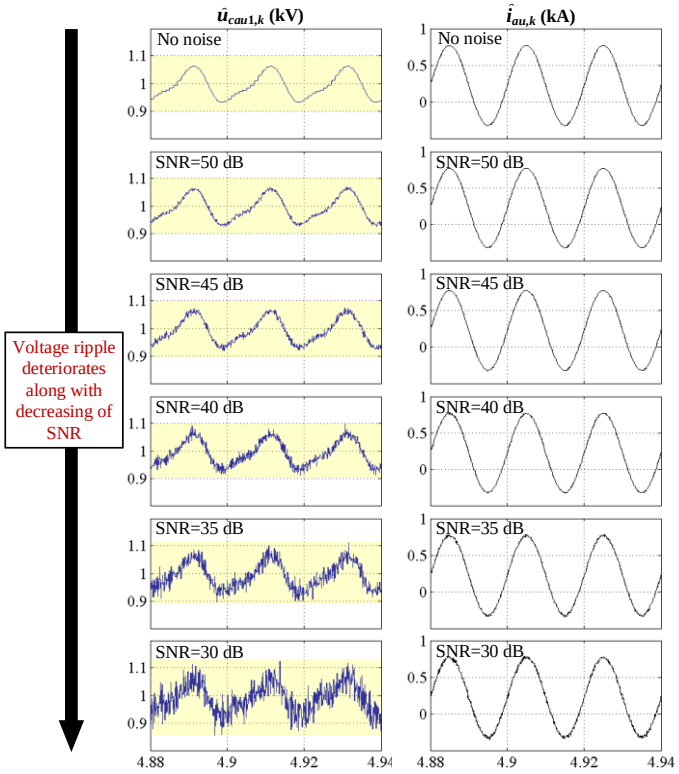

Fig. 6. Measured capacitor voltage and arm current under various SNRs.

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Fig. 6 shows the capacitor voltage $\hat{u}_{caui,k}$ and arm current $\hat{i}_{au,k}$ under various SNR, which are derived from case I in Section V with active power of 0.8 p.u. Here, the Gauss noise is superposed to the ideal capacitor voltage and arm current to simulate the random measurement error. In a practical system, the SNR is usually not less than 30 dB [37]. From Fig. 6, it can be observed that the noise has little effect on the arm current. However, the noise deteriorates the capacitor voltage ripple, because the capacitor voltage ripple is far smaller than the dc component in the capacitor voltage, such as typically 10% of the nominal dc component in capacitor voltage [38]. The noise deteriorates the capacitor voltage ripple along with decreasing of SNR. Consequently, it poses challenges to capacitance monitoring based on the capacitor voltage ripple.

To implement the proposed capacitance monitoring algorithm for the *i*-th SM in the discrete-time DSP controller with sampling step T_s, (11) and (13) are discretized as

$$\begin{cases} A_{u\_aui} = T_s \sum u_{caui,k} \cdot \cos(\theta_k) \\ B_{u\_aui} = T_s \sum u_{caui,k} \cdot \sin(\theta_k) \end{cases}, \tag{19}$$

$$\begin{cases} A_{i\_aui} = T_s \sum i_{au,k} \cdot y_{aui,k} \cdot \cos(\theta_k) \\ B_{i\_aui} = T_s \sum i_{au,k} \cdot y_{aui,k} \cdot \sin(\theta_k) \end{cases}, \tag{20}$$

Substituting (16) into (19) and (20), the $\hat{A}_{u\_aui}$, $\hat{B}_{u\_aui}$ corresponding to capacitor voltage and the $\hat{A}_{i\_aui}$, $\hat{B}_{i\_aui}$ corresponding to capacitor current can be obtained as

$$\begin{cases} \hat{A}_{u\_aui} = A_{u\_aui} + T_s \sum v_{i,k} \cos(\theta_k) \\ \hat{B}_{u\_aui} = B_{u\_aui} + T_s \sum v_{i,k} \sin(\theta_k) \end{cases} \tag{21}$$

$$\begin{cases} \hat{A}_{i\_aui} = A_{i\_aui} + T_s \sum w_k \cdot y_{aui,k} \cos(\theta_k) \\ \hat{B}_{i\_aui} = B_{i\_aui} + T_s \sum w_k \cdot y_{aui,k} \sin(\theta_k) \end{cases}. \tag{22}$$

According to (17) and (21), the relative error e_r of $\hat{A}_{u\_aui}$ and $\hat{B}_{u\_aui}$ obey normal distribution as

$$\begin{cases} e_r(\hat{A}_{u\_aui}) = \dfrac{\hat{A}_{u\_aui} - A_{u\_aui}}{A_{u\_aui}} \sim N\left(0, \sigma_v^2 T_s^2 \sum \left(\dfrac{\cos\theta_k}{A_{u\_aui}}\right)^2\right) \\ e_r(\hat{B}_{u\_aui}) = \dfrac{\hat{B}_{u\_aui} - B_{u\_aui}}{B_{u\_aui}} \sim N\left(0, \sigma_v^2 T_s^2 \sum \left(\dfrac{\sin\theta_k}{B_{u\_aui}}\right)^2\right) \end{cases}. \tag{23}$$

According to (17) and (22), the relative error e_r of $\hat{A}_{i\_aui}$ and $\hat{B}_{i\_aui}$ obey normal distribution as

$$\begin{cases} e_r(\hat{A}_{i\_aui}) = \dfrac{\hat{A}_{i\_aui} - A_{i\_aui}}{A_{i\_aui}} \sim N\left(0, \sigma_w^2 T_s^2 \sum \left(\dfrac{y_{aui,k}\cos\theta_k}{A_{i\_aui}}\right)^2\right) \\ e_r(\hat{B}_{i\_aui}) = \dfrac{\hat{B}_{i\_aui} - B_{i\_aui}}{B_{i\_aui}} \sim N\left(0, \sigma_w^2 T_s^2 \sum \left(\dfrac{y_{aui,k}\sin\theta_k}{B_{i\_aui}}\right)^2\right) \end{cases}. \tag{24}$$

According to (23) and (24), it can be observed that the means of $e_r(\hat{A}_{u\_aui})$, $e_r(\hat{B}_{u\_aui})$, $e_r(\hat{A}_{i\_aui})$ and $e_r(\hat{B}_{i\_aui})$ are zero respectively. In addition, A_{u_aui}, B_{u_aui}, A_{i_aui} and B_{i_aui} are located at denominator of the variance of $e_r(\hat{A}_{u\_aui})$, $e_r(\hat{B}_{u\_aui})$, $e_r(\hat{A}_{i\_aui})$ and $e_r(\hat{B}_{i\_aui})$, which would increase along with the increase of monitoring periods N_T, and therefore the variance of $e_r(\hat{A}_{u\_aui})$, $e_r(\hat{B}_{u\_aui})$, $e_r(\hat{A}_{i\_aui})$ and $e_r(\hat{B}_{i\_aui})$ are reduced along with increasing of N_T according to (11) and (13). As a result, $\hat{A}_{u\_aui}$, $\hat{B}_{u\_aui}$, $\hat{A}_{i\_aui}$ and $\hat{B}_{i\_aui}$ would be close to A_{u_aui}, B_{u_aui}, A_{i_aui} and B_{i_aui}, respectively, along with the increase of N_T, and therefore the impact of noise can be relieved during the accumulation process in the proposed capacitor monitoring strategy.

B. Selection of Monitoring Periods N_T

According to (23) and (24), the monitoring period N_T is important in the proposed capacitance monitoring strategy, which would affect the effect of noise immunity. Fig. 7(a) shows the average error of the proposed method with active power of 0.8 p.u. under various N_T and various SNR of the measurements, which are derived from the simulation in case I of Section V. Fig. 7(b) shows the average error with SNR=30 dB under various N_T and various active power. It can be observed that the average error of the proposed strategy would decrease along with the increase of N_T. When N_T is greater than 50, the increase of N_T would not contribute much to the decrease of the capacitance monitoring error. Consequently, to make a tradeoff between the accuracy and time consumption, N_T can be selected as 50 for the simulated system in Section V, which takes about one second for capacitance monitoring for each SM. For the MMC with 6 SMs per arm in the simulation studies in Section V, it requires about 36 s to complete capacitance monitoring once. Since the capacitor aging is a long-time effect [27], the variation of capacitance in a monitoring period can be neglected, which would not affect the accuracy of capacitance monitoring.

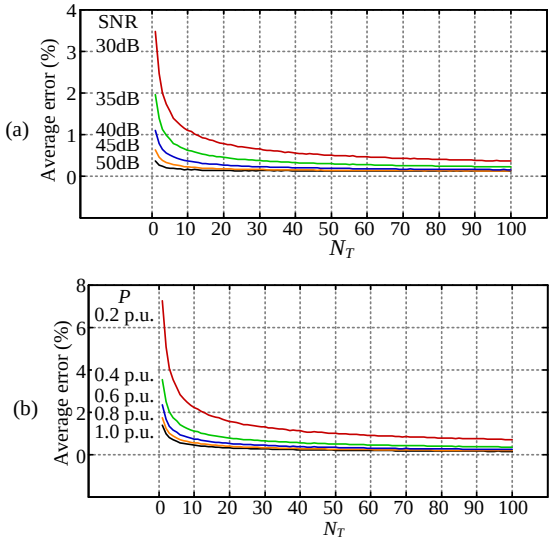

Fig. 7. Average error of the estimated capacitance. (a) P=0.8 p.u. under various N_T and various SNRs of measured capacitor voltage and arm current. (b) SNR=30 dB under various N_T and various active power.

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C. Comparison of Capacitance Monitoring Methods

Table I shows a comparison of the proposed monitoring method and existing methods [15], [17], [24], [27]. The proposed capacitance monitoring strategy only requires capacitor voltage, arm current and reference, but not precise SM switching function. As a result, the proposed strategy can be directly implemented in the DSP controller with a simple algorithm. However, the methods in [15], [17] and [24] require precise SM switching function, which requires the DSP to receive precise SM switching states from FPGA. They bring the difficulty for the DSP to have such a high sampling speed to receive precise SM switching states from FPGA and handle such a large calculation amount.

The average error of capacitance monitoring with the proposed method and those methods in [15], [17], [24] and [27] under various SNRs of sampled capacitor voltage and arm current are shown in Fig. 8, which are derived from the simulated system in case I of Section V. It can be observed that the capacitance estimation errors in [24] and [27] are obviously increased along with the decrease of SNR, while the capacitance estimation errors in [15], [17] and the proposed method are nearly not affected by the SNR because the proposed method and the methods in [15], [17] are highly immune to noise, which greatly reduce the demands on the quality of sensors.

In comparison with other methods, the proposed method is more adaptive and has no effect on the performance of the MMC. However, the method in [15] requires to inject the ac current into the circulating current and the method in [17] is only suitable for the MMCs without CCSC, which both increase the arm current and power losses. The method in [24] requires the monitored SM and the reference SM have the same switching function, which affects the capacitor voltage balancing control. The method in [27] requires the monitored SM to be bypassed and discharged through the bleeding resistor, and other SMs are required to be operated with increased capacitor voltage.

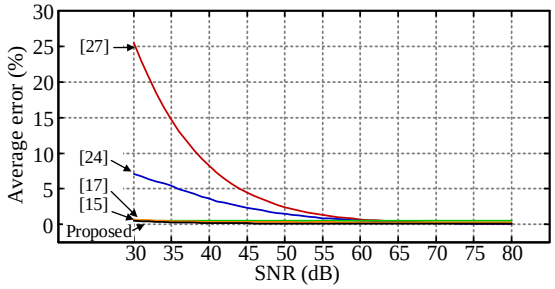


Fig. 8. Average error of the capacitance monitoring with different methods under various SNRs of measured capacitor voltage and arm current.

TABLE I
Comparison of the state-of-art capacitance monitoring methods for MMCs

Method	Implementation	Noise immunity	Effects on Performance
Ref. [27]	Simple	No	Yes
Ref. [24]	Difficult (require switching state)	No	Yes
Ref. [17]	Difficult (require switching state)	Yes	Yes
Ref. [15]	Difficult (require switching state)	Yes	Yes
Proposed method	Simple	Yes	No

Based on the above comparisons, the proposed capacitance monitoring method would be a better candidate for the PSC-PWM based MMC with the advantages of simple implementation, noise immunity and no effect on the control performance.

V. Simulation Studies

To verify the proposed capacitance monitoring strategy, a three-phase MMC system, as shown in Fig. 9, is simulated with PSCAD/EMTDC. In the simulation, the capacitors in upper arm of phase A are monitored. The capacitance C_{au5} and C_{au6} drops as C_{au5}=7.2 mF, C_{au6}=6.4 mF. The active power P and reactive power Q are 4 MW (0.8 p.u.) and 0 MVar, respectively. The system parameters are shown in Table II.

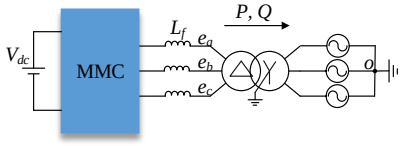


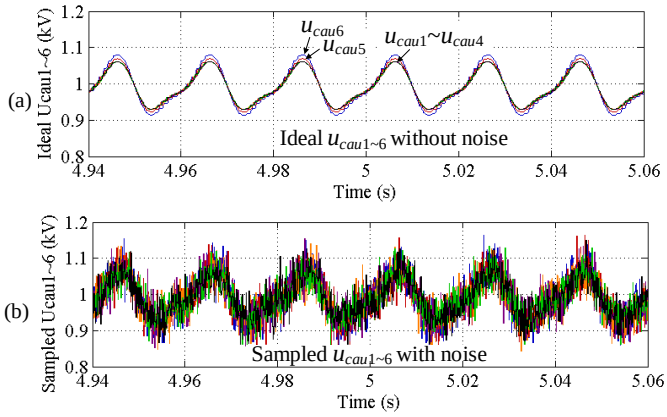
Fig. 9. Diagram of the simulated MMC system.

TABLE II
System Parameters for Simulation

Parameter	Value
Rated power	5 MVA
DC link voltage V_{dc}	6 kV
Grid line-to-line voltage	33 kV
Rated frequency f_0	50 Hz
Transformer voltage rating	3 kV/33 kV
Transformer leakage reactance	10%
Number of SM per arm N	6
Rated SM capacitance	8 mF
Arm inductance L_s	3 mH
Filter inductance L_f	1 mH
Carrier frequency	1 kHz
Sampling step T_s	100 us
SNR of system	30 dB
N_T	50

A. Case I: Monitoring under P=0.8 p.u. & Q=0

Figs. 10 (a) and (b) show the ideal capacitor voltages without noise and the sampled capacitor voltages with noise, respectively. Figs. 11 (c) and (d) show the ideal upper arm current without noise and the sampled upper arm current with noise. It can be observed that due to the large dc components in the capacitor voltages, the ripple components are more seriously affected by the sensor noise than the arm current. Besides, the voltage ripple of the SM with reduced capacitance is greater than the SM with rated capacitance.



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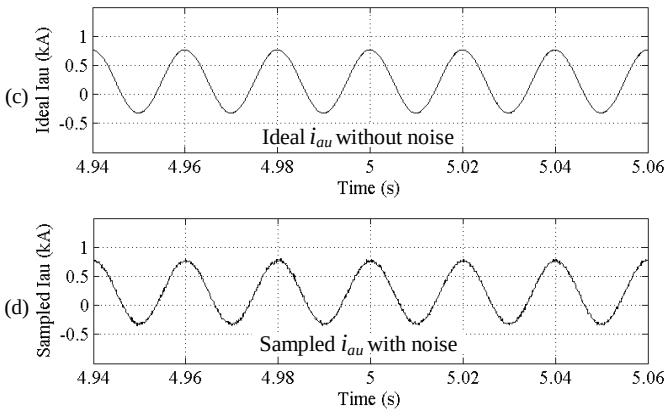


Fig. 10. Simulation results under rated condition. (a) Ideal u_{cau1}~u_{cau6}. (b) Sampled u_{cau1}~u_{cau6} with 30 dB noise. (c) Ideal i_{au}. (d) Sampled i_{au} with 30 dB noise.

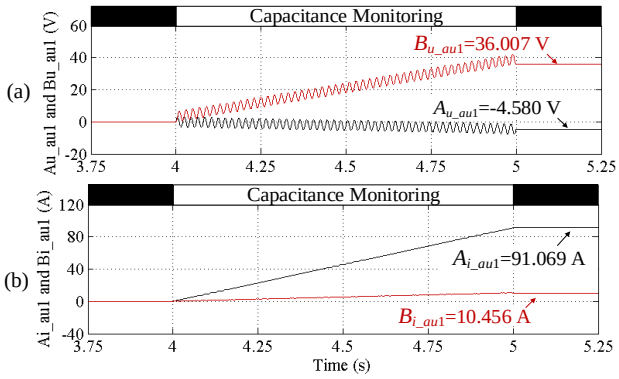


Fig. 11. Simulation result under rated condition. (a) A_{u_au1} and B_{u_au1} (b) A_{i_au1} and B_{i_au1}.

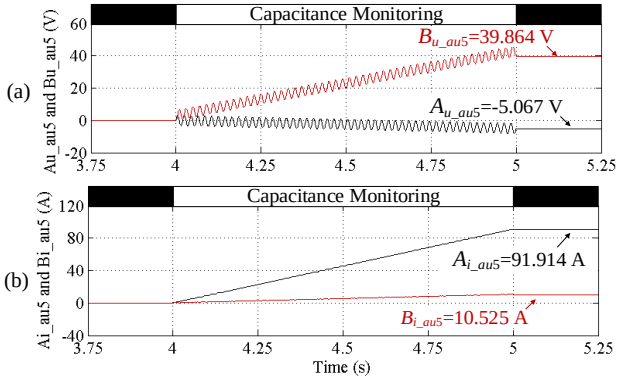


Fig. 12. Simulation results under rated condition. (a) A_{u_au5} and B_{u_au5} (b) A_{i_au5} and B_{i_au5}.

The performance of the proposed method for SM 1 with rated capacitance is shown in Fig. 11. Fig. 11(a) shows the integral process of A_{u_au1} and B_{u_au1}. Fig. 11(b) shows the integral process of A_{i_au1} and B_{i_au1}. The capacitor monitoring begins at t=4 s. Then, the amplitude of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} increase along with execution of the capacitance monitoring process. At t=5 s, the capacitance monitoring ends and C_{au1} is estimated as 8.039 mF with (12), (14) and (15).

The performance of the proposed method for SM 5 with reduced capacitance is shown in Fig. 12. Fig. 12(a) shows the integral process of A_{u_au5} and B_{u_au5}. Fig. 12(b) shows the integral process of A_{i_au5} and B_{i_au5}. The capacitance monitoring begins at t=4 s. Then, the amplitude of A_{u_au5}, B_{u_au5}, A_{i_au5} and B_{i_au5} increase along with the execution of the capacitance monitoring process. In comparison with the results of SM 1, as shown in Fig. 11, the amplitudes of A_{u_au5} and B_{u_au5} are respectively greater than the A_{u_au1} and B_{u_au1}, because the voltage ripple of SM 5 is greater than the voltage ripple of SM 1 due to the reduced capacitance, as shown in Fig. 10(a). At t=5 s, the capacitor monitoring ends and C_{au5} of SM 5 is estimated as 7.250 mF.

The SMs in upper arm of phase A are estimated one by one by the proposed capacitance monitoring strategy. The estimated capacitance C_{au1}~C_{au6} are shown in Fig. 13(a) and the errors of the estimation are shown in Fig. 13(b), where the maximum error is 0.69%.

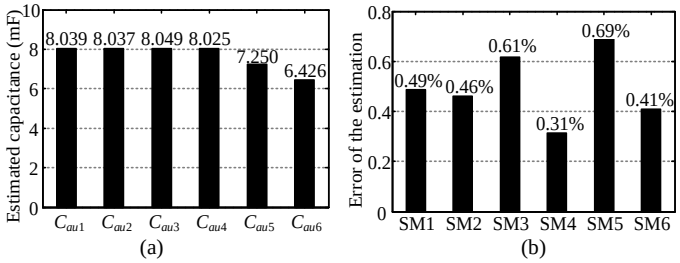


Fig. 13. Simulation results under rated condition. (a) Estimated capacitance C_{au1}~C_{au6}. (b) Errors of estimated capacitance.

B. Case II: Monitoring with Low Switching Frequency

Fig. 14 shows the performance of the MMC with low switching frequency, where the SM switching frequency is 250 Hz. Figs. 14(a) and (b) show the ideal capacitor voltages without noise and the sampled capacitor voltages with noise, respectively. Figs. 14 (c) and (d) show the ideal upper arm current without noise and the sampled upper arm current with noise.

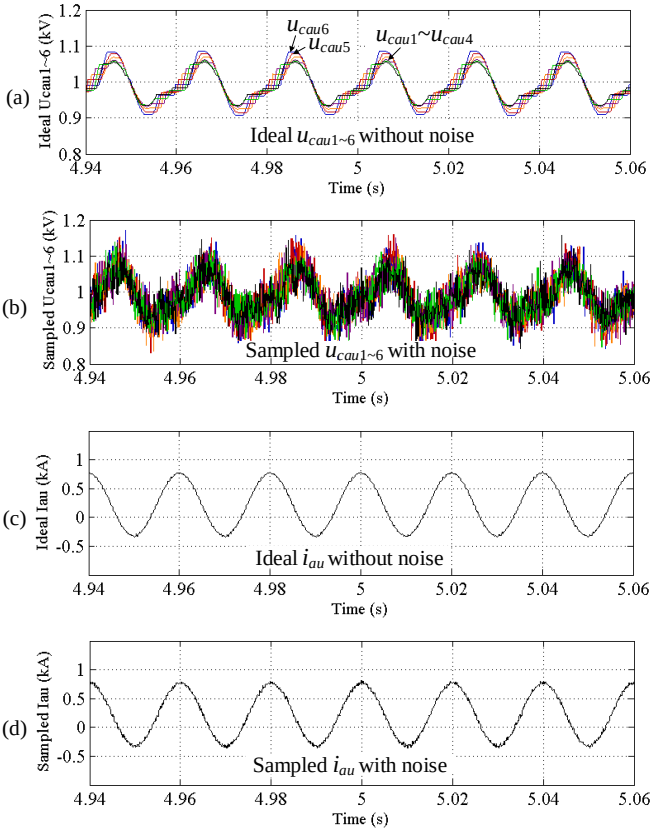


Fig. 14. Simulation results with low switching frequency. (a) Ideal u_{cau1}~u_{cau6}. (b) Sampled u_{cau1}~u_{cau6} with 30 dB noise. (c) Ideal i_{au}. (d) Sampled i_{au} with 30 dB noise.

The estimated capacitance C_{au1}~C_{au6} in upper arm of phase A are shown in Fig. 15(a) and the errors of the estimation are shown in Fig. 15(b), where the maximum error is 0.58%. In comparison with the results in case I, the estimation error is not increased due to the reduced switching frequency.

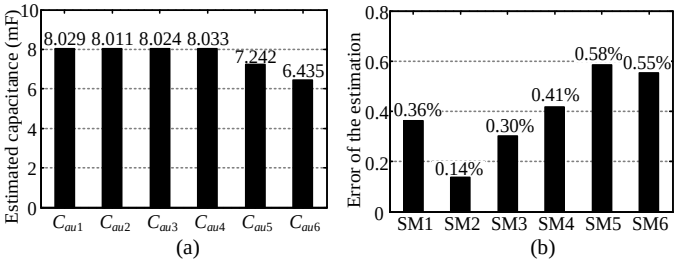


Fig. 15. Simulation results with low switching frequency. (a) Estimated capacitance C_{au1}~C_{au6}. (b) Errors of estimated capacitance.

Fig. 16 shows the average error of the proposed capacitance monitoring method under various switching frequencies and various SNRs. It can be observed that the average error almost remains constant under various switching frequencies and the average error is decreased along with the increase of the SNR.

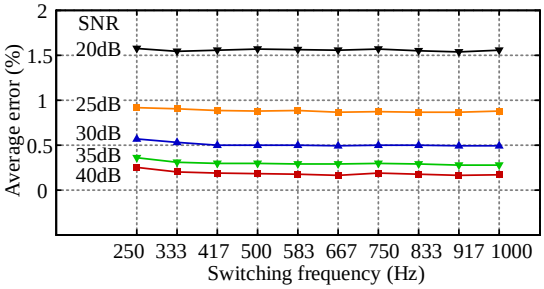


Fig. 16. Average error of the proposed method under various switching frequencies and various SNRs.

VI. Experimental Studies

A three-phase MMC is built in laboratory to confirm the proposed strategy. A photo of experimental setup is shown in Fig. 17. A dc source SGA600/10 is adopted to support the dc link voltage and a voltage regulator is adopted to support the ac voltage. The output current control [39], CCSC [32] and capacitor voltage balancing control [31] are implemented in the DSP TMS320F28346, while the FPGA XC6SLX16 is adopted to achieve the PSC-PWM scheme and generate the driver signals. Then, the pulse signals are transferred to each SM via optical fiber. The voltage sensors LEM LV25-P [40] are equipped to convert the capacitor voltage to voltage signal while the current sensors LEM LA55-P [41] are equipped to convert the arm current to voltage signal. And the voltage signals are sampled by the analog-digital converter (ADC). The system parameters are listed in TABLE III.

To verify the proposed capacitance monitoring strategy, the small capacitances C_{au3} and C_{au4} are adopted, where manufacture parameters are given as 1.88 mF and 1.41 mF, respectively. The proposed scheme is implemented in the DSP controller, and the internal signals A_{u_aui}, B_{u_aui}, A_{i_aui} and B_{i_aui} are output by the digital-analog converter (DAC) and recorded by an oscilloscope, while the capacitance monitoring results are directly transferred from the DSP controller to the host computer through Transmission Control Protocol (TCP) based Ethernet.

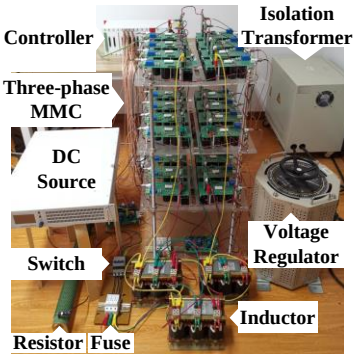


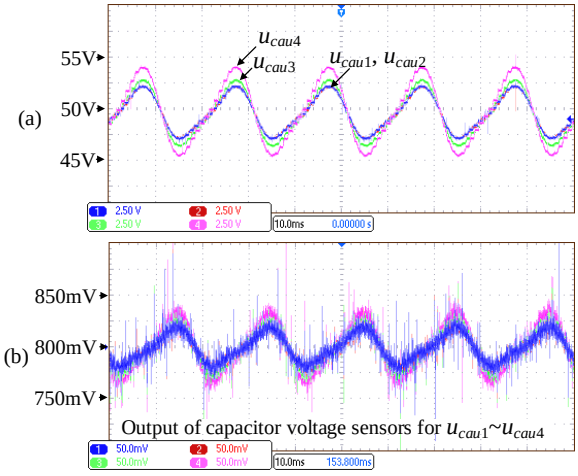
Fig. 17. Photo of the experimental MMC system.

TABLE III
Parameters for Three-Phase MMC Experimental System

Parameter	Value
Rated Power	1 kW
DC link voltage V_{dc}	200 V
AC line-to-line voltage	100 V
Rated frequency f_0	50 Hz
Number of SM per arm N	4
Rated SM capacitance	2.35 mF
Arm inductance L_s	3 mH
Filter inductance L_f	3 mH
Carrier frequency	1 kHz
Sampling step T_s	100 us

A. Case I: Monitoring under P=0.8 p.u. & Q=0

Fig. 18 shows the performance of the MMC, where the power with active power of 0.8 p.u. and reactive power of 0 p.u. are transferred from dc side to ac side. Fig. 18(a) shows the capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A, which are obtained by voltage probes with 50 kHz low-pass filter. Fig. 18(b) shows the output voltages of capacitor voltage sensors for u_{cau1}~u_{cau4} by the voltage probes with full bandwidth. The ripples of u_{cau3} and u_{cau4} are greater than those of u_{cau1} and u_{cau2} due to the reduced C_{au3} and C_{au4}. Fig. 18(c) shows the arm currents i_{au} and i_{al}, which are obtained from the arm circuit by the current probes with a 50 kHz low-pass filter. Fig. 18(d) shows the output voltages of current sensors for i_{au} and i_{al} by the voltage probes with full bandwidth. It can be observed that the measured capacitor voltages and arm currents through sensors are affected by noise. Owing to that the capacitor voltage ripple accounts for a small part in capacitor voltage, the capacitor voltage ripple measured from voltage sensors are more seriously affected by the noise than the arm current.



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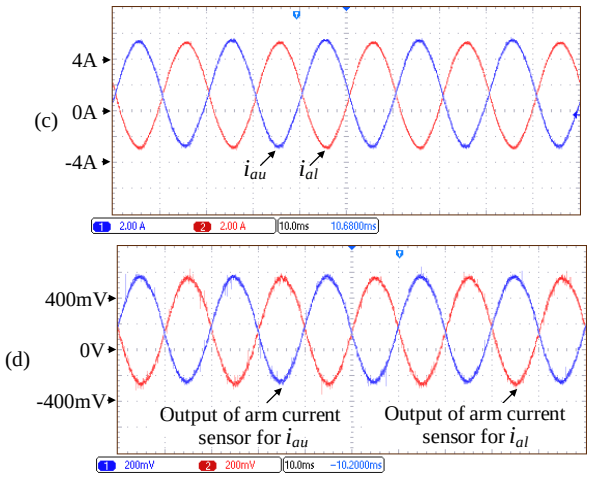

Fig. 18. Experimental results under rated condition. (a) u_{cau1}~u_{cau4}. (b) Output of capacitor voltage sensors for u_{cau1}~u_{cau4}. (c) i_{au} and i_{al}. (d) Output of current sensors for i_{au} and i_{al}. Time base is 10 ms/div.

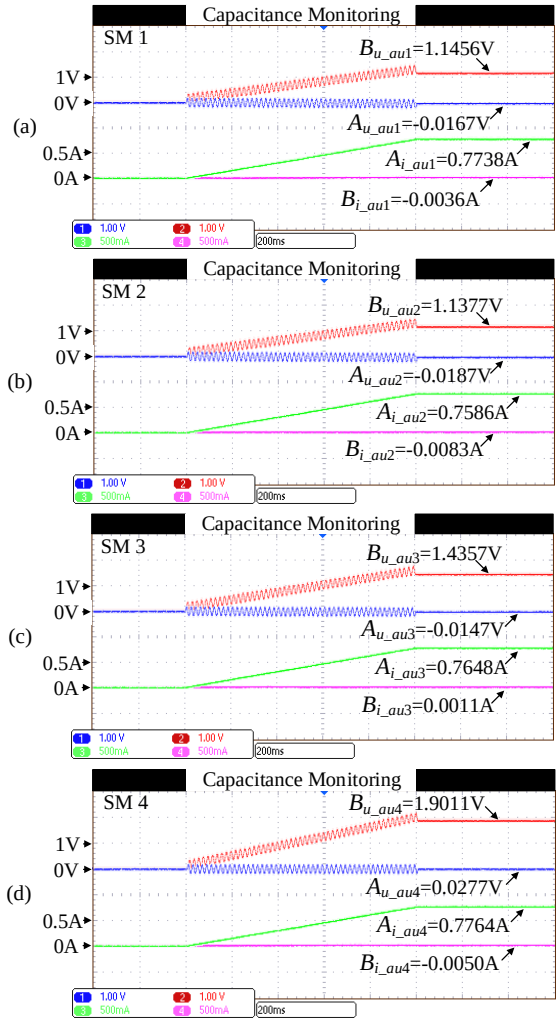

Fig. 19. Experimental results under rated condition. (a) A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} for SM 1. (b) A_{u_au2}, B_{u_au2}, A_{i_au2} and B_{i_au2} for SM 2. (c) A_{u_au3}, B_{u_au3}, A_{i_au3} and B_{i_au3} for SM 3. (d) A_{u_au4}, B_{u_au4}, A_{i_au4} and B_{i_au4} for SM 4. Time base is 200 ms/div.

The performance under the proposed capacitance monitoring strategy is shown in Fig. 19. Fig. 19(a) shows the integral process of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} for SM 1, where the amplitude of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} increase along with execution of the capacitance monitoring process. Afterwards, C_{au1} is estimated to be 2.150 mF. Figs. 19 (b), (c) and (d) show the integral process for SM 2, SM 3 and SM 4, respectively.

Fig. 20(a) shows the estimated capacitance with proposed scheme and the measured capacitance using the UNI-T UT612 LCR meter. Fig. 20(b) shows the relative errors between estimated capacitance and the measured capacitance, where the maximum error is 0.59%.

Fig. 21 shows the estimated capacitance of SM 1 under various active power from 0.2 p.u. to 1.0 p.u., where the proposed capacitance monitoring strategy is conducted forty times for each case. It can be observed that along with the increase of the active power, the proposed strategy shows reduced errors. In most of the cases, the error of the estimated capacitance is less than 1%.

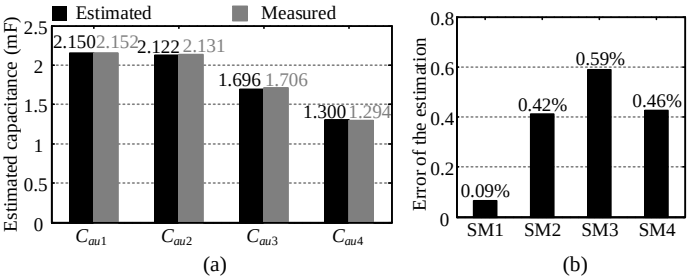

Fig. 20. Experimental results under rated condition. (a) Estimated capacitance C_{au1}~C_{au4}. (b) Errors of estimated capacitance.

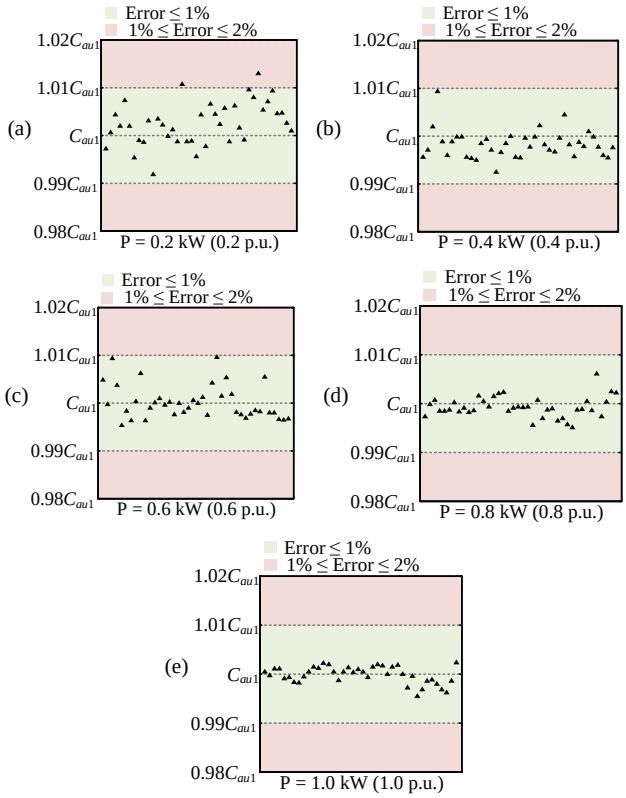

Fig. 21. Estimated capacitance of SM 1 under various active power operation. (a) 0.2 p.u. (b) 0.4 p.u. (c) 0.6 p.u. (d) 0.8 p.u. (e) 1.0 p.u.

B. Case II: Monitoring with Low Switching Frequency

Fig. 22 shows the performance of the MMC, where the switching frequency for each SM is 390 Hz. Fig. 22(a) shows the capacitor voltages u_{cau1}~u_{cau4} in the upper arm of phase A. Fig. 22(b) shows the output voltages of the capacitor voltage

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sensors for u_{cau1}~u_{cau4}. The ripples of u_{cau3} and u_{cau4} are greater than those of u_{cau1} and u_{cau2} due to the reduced C_{au3} and C_{au4}. Fig. 22(c) shows the upper arm current i_{au} and the lower arm current i_{al}. Fig. 22(d) shows the output voltages of current sensors for i_{au} and i_{al}. The arm currents are slightly distorted due to the low switching frequency.

Fig. 23(a) shows the estimated capacitance with proposed scheme and the measured capacitance using the UNI-T UT612 LCR meter. Fig. 23(b) shows the relative errors between estimated capacitance and the measured capacitance, where the maximum error is 0.54%. In comparison with the results in case I, the estimation error is not increased due to the low switching frequency.

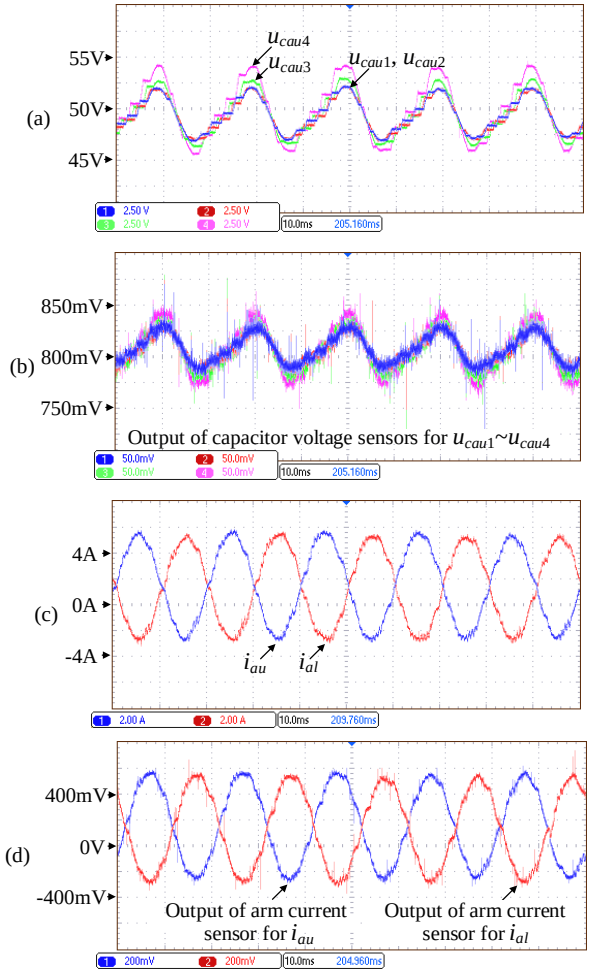

Fig. 22. Experimental results with low switching frequency. (a) u_{cau1}~u_{cau4}. (b) Output of capacitor voltage sensors for u_{cau1}~u_{cau4}. (c) i_{au} and i_{al}. (d) Output of current sensors for i_{au} and i_{al}. Time base is 10 ms/div.

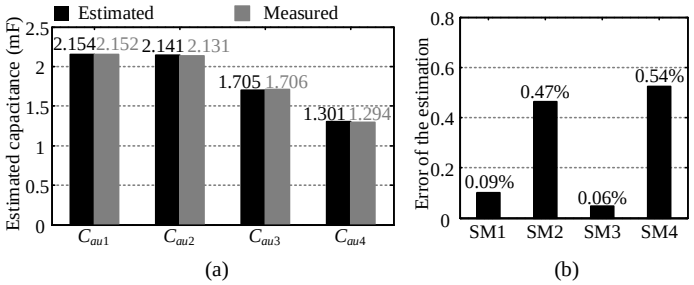

Fig. 23. Experimental results with low switching frequency. (a) Estimated capacitance C_{au1}~C_{au4}. (b) Errors of estimated capacitance.

C. Case III: Monitoring with Various Modulation Indexes

To test the performance of the proposed method under various modulation indexes, the ac-side voltage is changed so that the MMC can work with various modulation indexes. The estimated capacitance and relative error for SM 2 with proposed method under various modulation indexes are listed in TABLE IV. It can be observed that the error of the estimation is lower than 1% when the modulation index is above 0.4. Normally, the modulation index is rarely low as 0.4 during normal operation in practical application.

TABLE IV
Experimental Results for SM 2 under Various Modulation Index

Modulation Index	Estimated Capacitance (mF)	Errors (%)
0.2	2.159	1.31
0.4	2.144	0.61
0.6	2.143	0.56
0.8	2.138	0.33

D. Case IV: Monitoring with Different Power Factors

To test the performance of the proposed method under different power factors, the apparent power of the MMC is kept at 0.8 p.u. and the power factor varies from 1 to 0. The estimated capacitances and relative errors for SM 2 under various power factors are listed in TABLE V. It can be observed that the accuracy of the estimated capacitance is almost not affected by the power factors.

TABLE V
Experimental Results for SM 2 under Various Power Factors

Power Factor	Estimated Capacitance (mF)	Errors (%)
1.0	2.139	0.38
0.8	2.145	0.66
0.6	2.138	0.33
0.4	2.134	0.14
0.2	2.127	0.19
0	2.136	0.23

E. Case V: Monitoring with Different Load Frequency

To test the performance of the proposed method under different load frequency, the MMC with filter inductor and resistor load of 10 Ω is adopted and the load frequency is 25 Hz.

Fig. 24 shows the integral process of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} for SM 1 and C_{au1} is estimated to be 2.153 mF. Because of the reduced load frequency, the monitoring time is prolonged to about 2 s in comparison with the case I.

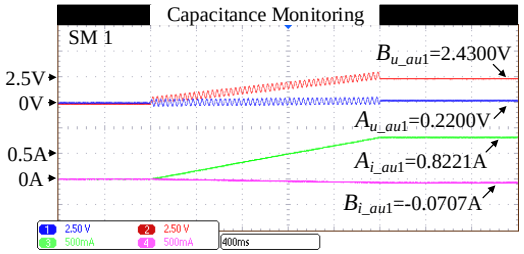

Fig. 24. Experimental results of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} for SM 1 with load frequency of 25 Hz. Time base is 400 ms/div.

Fig. 25(a) shows the estimated capacitance with proposed scheme and the measured capacitance using the UNI-T UT612 LCR meter. Fig. 25(b) shows the relative errors between estimated capacitance and the measured capacitance, where the maximum error is 0.54%.

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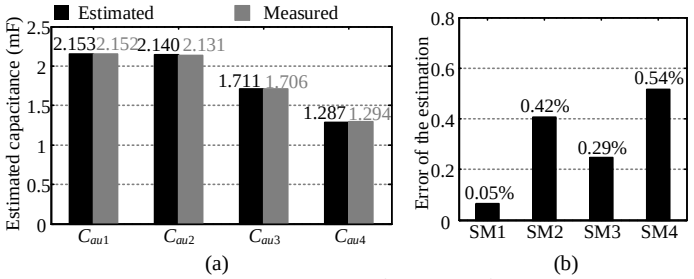

Fig. 25. Experimental results with load frequency of 25 Hz. (a) Estimated capacitance C_{au1}~C_{au4}. (b) Errors of estimated capacitance.

F. Case VI: Monitoring with Arm Inductor Mismatch

To test the performance of the proposed capacitor monitoring method under arm inductor mismatch, the arm inductor in the upper arm of phase A is 1.5 mH and the arm inductors in other arms are 3 mH.

Fig. 26(a) shows the estimated capacitance with proposed scheme and the measured capacitance using the UNI-T UT612 LCR meter. Fig. 26(b) shows the relative errors between estimated capacitance and the measured capacitance, where the maximum error is 0.7%.

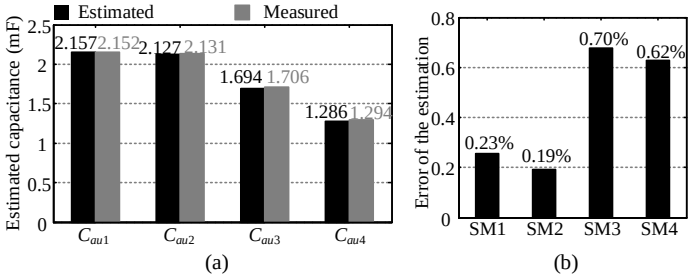

Fig. 26. Experimental results with arm inductor mismatch. (a) Estimated capacitance C_{au1}~C_{au4}. (b) Errors of estimated capacitance.

G. Case VII: Monitoring with Increased Capacitance

To test the performance of the proposed capacitance method with increased capacitance, the SM 1 with larger capacitance is adopted and the capacitance is measured as 2.616 mF using the UNI-T UT612 LCR meter.

Fig. 27 shows the integral process of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} for SM 1, where the amplitude of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} increase along with execution of the capacitance monitoring process. Afterwards, C_{au1} is estimated to be 2.598 mF and the estimation error is 0.69%.

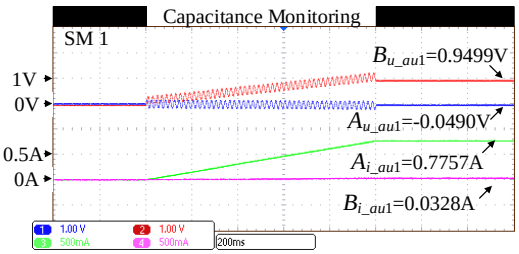

Fig. 27. Experimental results of A_{u_au1}, B_{u_au1}, A_{i_au1} and B_{i_au1} for SM 1 with increased capacitance. Time base is 200 ms/div.

H. Temperature Effect on Capacitance

The capacitance of the electrolytic capacitor also depends on the capacitor temperature. The capacitance increases along with the increase of the temperature due to the changing properties of the relative permittivity of the capacitor's dielectric material [42]. In order to determine the relationship between capacitance and temperature of the capacitor, the temperature chamber is used to keep the capacitor temperature constant and the capacitance is measured by LCR meter. Fig. 28 shows the photo of the experimental system.

Fig. 29 shows the measured capacitance of five capacitor samples under various temperature from 25 °C to 85 °C. The measured results of five samples are fitted with linear model [43], respectively, as plotted in Fig. 29. The corresponding coefficient of determination R^2 of fit is adopted to evaluate the effectiveness of the linear fit. In Fig. 29, the minimum R^2 of the fitting results is 99.62%, which proves that the relationship between capacitance and temperature can be fitted well by the linear model. The average value (dash line) of the five fit results is also plotted in Fig. 29 and the slope of the average value is 1.73 uF/°C. With the capacitance estimated by the proposed capacitance monitoring method and the capacitor temperature, the capacitance at 25 °C can be obtained based on the slope of the average value of these fit results. And then, the capacitor is judged to be failed if its capacitance at 25 °C is less than the threshold value.

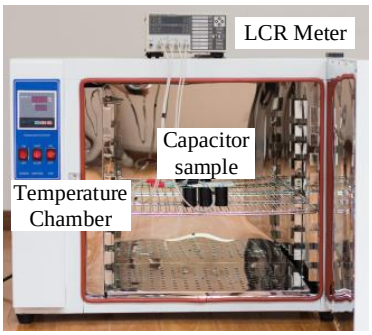

Fig. 28. Photo of the experimental system.

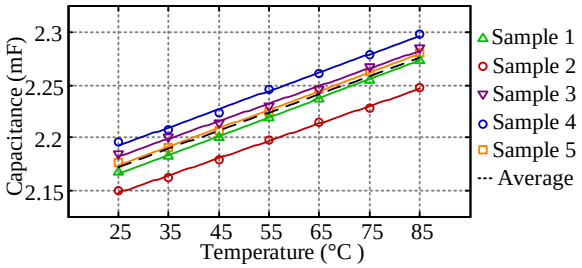

Fig. 29. The measured capacitance of five samples under various temperatures and their fitting results.

VII. Conclusion

This paper presents a submodule capacitance monitoring strategy for PSC-PWM based MMC, where the fundamental frequency components of the SM capacitor voltage and current are extracted to estimate the SM capacitance based on the reference, but do not need the precise switching states. The proposed scheme not only simplifies the implementation and calculations, but also avoids heavy communication burden between DSP and FPGA as well as extra control or any effect on the control performance. In addition, the impact of noise is also analyzed, where the proposed monitoring strategy can eliminate noise impact from sensors and increase accuracy. Simulation and experimental studies are also implemented, and the results confirm the effectiveness of the proposed strategy.

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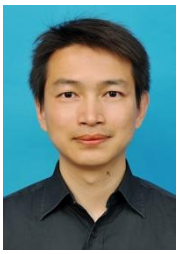

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